Attorney's Docket No.: 10559-773001 / P13943

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : David C. Chalupsky et al.
Serial No. : 10/081,658
Filed : February 22, 2002
Title : AUTOMATIC POWER DOWN

Art Unit : 2181
Examiner : Unknown

Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

I, Thomas Stachura, one of the inventors for the above-referenced application, am aware of a power management system employed by a Fast Ethernet controller made by Intel Corp. which I believe was in use prior to one year before the filing date of the above-referenced application. I am not aware of any documentation which describes this power management system.

I believe that the power management system of the Fast Ethernet controller has three power management states, D0a, D0u, and D3. These three power management states are defined in the same manner as indicated in Table III of the application. The Fast Ethernet controller is configured to permit an operating system to write to a register located within the controller to change power states from D0a to D3 or from D3 to D0u. The Fast Ethernet controller also is enabled to monitor a bus reset signal, such as the PCI_RST# signal, and change power management states as a result of a change in that signal. Specifically, the Fast Ethernet controller goes to D0u if the PCI_RST# signal transitions from low to high. It then remains in D0u until memory access is enabled, at which time the controller transitions to the D0a state. The physical layer interface of the Fast Ethernet controller has two power states: on and off. The Fast Ethernet device may be configured to turn its physical layer on or off depending upon the power management state of the device and whether wake up has been enabled. The physical

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

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Signature

JONATHAN R EASTWOOD
Typed or Printed Name of Person Signing Certificate

layer interface is always on when the power management state of the device is in D0a irrespective of the wake up settings. If wake up is enabled and the Fast Ethernet controller is in the D3 or D0u state, the physical layer is on. If wake up is disabled and the Fast Ethernet controller is in the D3 or D0u state, then the physical layer is off.

Respectfully submitted,

Date: 7/16/2002

Thomas L. Stachura

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Attorney's Docket No.: 10559-773001 / P13943

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : David C. Chalupsky et al.
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Title : AUTOMATIC POWER DOWN

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Examiner : Unknown

Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Applicant submits the references listed on the attached form PTO-1449, copies of which are enclosed.

This statement is being filed within three months of the filing date of the application or before the receipt of a first Office Action on the merits. A check in the amount of $180 is enclosed for the submission of Information Disclosure Statement fee. Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/24/02

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Jonathan R Fastwood
Typed or Printed Name of Person Signing Certificate

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-773001	Application No. 10/081,658
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant David C. Chalupsky et al.	
		Filing Date February 22, 2002	Group Art Unit 2181

U.S. Patent Documents

Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	*Inventor's Information Disclosure Statement, July 16, 2002*
	AR	*PCI Local Bus Specification, Revision 2.2*, December 18, 1998
	AS	*PCI Bus Power Management Interface Specification, Revision 1.1*, December 18, 1998
	AT	*Advanced Configuration and Power Interface Specification, Revision 2.0*, July 27, 2000

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.